REMARKS

This paper is responsive to the Office action dated August 19, 2002, having a shortened statutory period expiring November 19, 2002 wherein,

Claims 1-29 were previously pending in the application; and

Claims 1-29 were rejected.

Claim 6 has been amended.

Accordingly, claims 1-29 remain currently pending in the present application.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **VERSION WITH MARKINGS TO SHOW CHANGES MADE.**

Examiner's Objections

In the present Office Action, the Examiner objected to Applicants' title and abstract. Applicants have amended the title and abstract of the disclosure as indicated herein and respectfully submit that the Examiner's objections have consequently been overcome.

Rejection of Claims under 35 U.S.C. §102

Claims 1-3, 6, 7, 13-17, 20-22, and 25-27 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,128,666, issued to Muller et al. (hereinafter, "***Muller***").

Rejection of Claims under 35 U.S.C. §103

Claims 1-7, 13-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Muller*** as applied to claims 1-3, 6, 7, 13-17, 20-22, and 25-27 above, and further in view of United States Patent No. 6,018,524 issued to Turner et al. (hereinafter, "***Turner***").

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Muller*** as applied to claim 6 above, and further in view of United States Patent No. 5,761,191 issued to VanDervort et al. (hereinafter, "***VanDervort***").

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Muller*** as applied to claim 6 above, and further in view of United States Patent No. 6,275,953 issued to Vahalia et al. (hereinafter, "***Vahalia***").

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Muller*** as applied to claim 6 above, and further in view of United States Patent No. 6,078,593 issued to Eames et al. (hereinafter "***Eames***").

While not conceding that the Examiner's cited references qualify as prior art, but instead to expedite prosecution, Applicants have chosen to overcome-in-part and respectfully disagree and traverse-in-part the Examiner's rejections as follows. The following amendments and arguments are made without prejudice to Applicants' right to establish, for example in a continuing application, that one or more of the Examiner's cited references do not qualify as prior art with respect to an invention embodiment currently or subsequently claimed.

Applicants' claim 1, as originally submitted, recites a method of packet processing comprising: "parsing a packet, said packet having a header portion, to determine a vector; coordinating processing using said vector; deconstructing said packet header to form header data; searching one or more data structures based on said header data to produce search results; editing said packet based on said search results, said header data, and said vector; wherein said coordinating further comprises monitoring said deconstructing, said searching, and said editing."

In the present Office Action, the Examiner states with respect to Applicants' claim 1 that, ***Muller*** teaches a method of packet processing (col. 1, lines 10-15) comprising: "Parsing a packet, said packet having a header portion, to determine a vector (col. 6, lines 5-10)."

Applicants respectfully submit that the Examiner has failed to make out a *prima facie* case of anticipation or obviousness and moreover that ***Muller*** fails to teach, show, or suggest all elements and/or limitations of Applicants' claim.

The Examiner's cited portion of ***Muller*** teaches, "Logic 314...is also included to forward control information and also replace predetermined fields of the header as the header is transmitted out of the IPP 310 and into the packet memory 325. The IPP 310 forwards a

copy of the header to the search engine 315 which searches the database 320 to determine **if there is** information relevant to the packet such as the type of packet, e.g., VLAN supported or whether the packet can be routed." (***Muller***, Column 6, Lines 2-10, emphasis supplied)

Applicants respectfully submit that it is unclear what specific part or parts of the above-quoted portion of ***Muller*** the Examiner intended to indicate as teaching, showing, or suggesting, "parsing a packet...to determine a vector" as claimed (Applicants' claim 1) and consequently that a *prima facie* case of neither anticipation nor obviousness has been made with respect to Applicants' claim 1.

Moreover, Applicants respectfully submit that neither forwarding "a copy of the header to the search engine 315" nor searching "the database 320 to determine if there is information relevant to the packet such as the type of packet," alone or in combination, teaches, shows, or suggests, "parsing a packet...to determine a vector" as claimed. (Applicants' claim 1, emphasis supplied)

Applicants' claim 6, as amended, recites an apparatus for packet processing, comprising: "a central processor for packet processing, said central processor comprising a register set; and one or more peripheral processors each connected to said central processor and each comprising a register set, wherein each said peripheral processor returns at least one datum to said central processor; wherein said central processor communicates with each said peripheral processor and said one or more peripheral processors comprises a packet parser to determine a vector."

In the present Office Action, the Examiner states with respect to Applicants' claim 6 that, ***Muller*** teaches an apparatus for packet processing, comprising: "One or more peripheral processors each connected to said central processor and each comprising a register set" (col. 3, lines 56-58).

Applicants respectfully submit that ***Muller*** fails to teach, show, or suggest all elements and/or limitations of Applicants' claim.

The Examiner's cited portion of ***Muller*** teaches, "a central processing system (CPS) 160 that is coupled to the individual subsystem 110 through a communication bus 151 such as the peripheral components interconnect (PCI)." (***Muller***, Column 3, Lines 55-58) According to the teaching of ***Muller***, the described subsystems each include "a switch element 111 coupled to a forwarding memory 113 and an associated memory 114" (***Muller***, Column 3, Lines 39-41) with each switch element in turn including "a central processing unit (CPU) interface, a switch fabric block, a network interface, a cascading interface, and a shared memory manager." (***Muller***, Column 4, Lines 1-4)

Applicants therefore respectfully submit that the Examiner's cited portion of ***Muller***, fails to teach, show, or suggest, "one or more peripheral processors...comprising a register set," (Applicants' claim 6, as originally submitted, emphasis added) "wherein...said one or more peripheral processors comprises a packet parser to determine a vector" (Applicants' claim 6, as amended, emphasis supplied) as claimed.

Applicants therefore respectfully submit that the Examiner's rejections of Applicants' claims 1 and 6 under 35 U.S.C. §102 and 35 U.S.C. §103 are improper and should be withdrawn. It is therefore respectfully submitted that Applicants' claims 1 and 6, are each independently allowable over the Examiner's cited reference, ***Muller***. Applicants' claims 15, 20, and 25, which include limitations substantially similar to those described with respect to Applicants' claim 1, and remaining claims 2-5, 7-14, 16-19, 21-24 and 26-29, which depend directly or indirectly from claims 1, 6, 15, 20 or 25, are similarly allowable for at least those reasons as stated for the allowability of those claims. Accordingly, Applicants submit that all currently pending claims are allowable and respectfully request withdrawal of the Examiner's outstanding rejections.

CONCLUSION

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5097.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Box: Non-Fee Amendment, Commissioner for Patents, Washington, D.C. 20231, on **November 6, 2002**.

Attorney for Applicant(s) — Date of Signature: 11-6-02

Respectfully submitted,

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Version with Markings to Show Changes Made

In the Title

The title of the invention has been amended as follows:

NETWORK PROCESSOR SYSTEM **INCLUDING A CENTRAL PROCESSOR AND AT LEAST ONE PERIPHERAL PROCESSOR**

In the Abstract

The abstract of the disclosure has been amended as indicated below:

[**The present invention consists of a**] **A** general purpose, software-controlled central processor (CP) **can be** augmented by a set of task specific, specialized peripheral processors (PPs). The central processor accomplishes its functions with the support of the PPs. Peripheral processors may include but are not limited to a packet parser, [**which provides the central processor with a numerical summary of the packet format;**]a packet deconstructor, [**which extracts designated fields from the packet the positions of which are determined by the central processor according to the packet format;**]a search engine, [**which is supplied a lookup index by and returns its results to the central processor;**]and a packet editor[**which modifies the packet as determined by the central processor using (in part) information returned from other peripherals**]. At each step in the use of this network processor system, the central processor has an opportunity to intervene and modify the handling of the packet based on its interpretation of PP results. The programmable nature of the CP and the PPs provides the system with flexibility and adaptability[**: rather than having to modify a circuit or system design in an ASIC or other hardware, new packet processing applications may be accommodated through the development of new software and its deployment in the central and/or peripheral processors**].

In the Claims

6. (**Amended Once**) An apparatus for packet processing, comprising:

a central processor for packet processing, said central processor comprising a register set; and

one or more peripheral processors each connected to said central processor and each comprising a register set, wherein each said peripheral processor returns at least one datum to said central processor;

wherein said central processor communicates with each said peripheral processor **and said one or more peripheral processors comprises a packet parser to determine a vector**.